Short Papers

An Investigation of the High-Frequency Limit of a Miniaturized Commercial Voltage-Controlled Oscillator Used in 900-MHz-Band Mobile-Communication Handset

Kyung-Whan Yeom

***Abstract*—The 900–MHz-band voltage-controlled oscillator (VCO) currently used in a commercial mobile-communication handset has the features of light weight, small size, low phase noise, and low dc current consumption. This paper investigates the problems that may occur when these types of VCO's are employed in next-generation high-frequency mobile-communication handsets. The results show that oscillation may not commence above frequency $f_T/2\sqrt{R_{eq}/r_{bb}}$, which is significantly below the $f_{\max}$ of the device itself, due to the effects of the circuit elements. In addition, a new formula is proposed which provides a practical guideline for selection of the active devices. The procedure for extraction of the small-signal model required by the proposed formula is also described in detail. The results obtained with the formula are in good agreement with those obtained from the measured S-parameters.**

***Index Terms*—Maximum frequency of oscillation, mobile communication VCO.**

I. Introduction

The demand for mobile communication is increasing rapidly and the new mobile communication service, called a personal communication system (PCS) [1], utilizing a 2-GHz spectrum is emerging. In this system, voltage-controlled oscillators (VCO's) are used as components of frequency synthesizers, which provide a choice of the desired channel.

In such an application, a VCO must exhibit low phase noise, very low dc current consumption (in order to lengthen the time between battery recharges), and low voltage operation to reduce the number of battery cells. For portability, the VCO should have both small size and light weight. Furthermore, it should have a surface-mountable structure for ease of assembly in handset production.

The VCO structure, shown in Fig. 1, has been widely used [2], [3] in 900-MHz handheld phones. It consists of a thin metal cover providing electromagnetic shielding and a multilayer printed circuit board (PCB) with a sectional view, shown in Fig. 2. The multilayer PCB provides several terminals for interfacing with an external PCB. The bottom metallization layer of this PCB is a ground layer. However, except for solderable terminals, most of this layer is coated with solder resist to insulate it from the external PCB.

The multilayer PCB usually consists of four metalized layers, equally spaced, with dielectric material, as shown in Fig. 2. Circuit elements are mounted on the top metallization layer, while the second and fourth metallization layers serve as the grounds. Elements, such as the resonator θ_1 and transmission lines TL_1 and TL_2 (shown in Fig. 3) are usually located in the third metallization layer using stripline technology. Very often, VCO size can be reduced further by use of smaller chip resistors and capacitors, such as the 1005 style (the width and length are 0.5 and 1.0 mm, respectively).

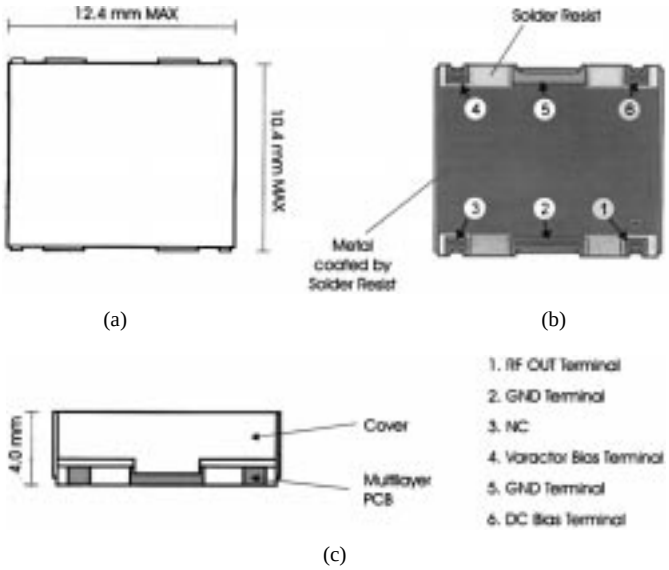

Fig. 1. Structure of a VCO. (a) Top view. (b) Bottom view. (c) Front view.

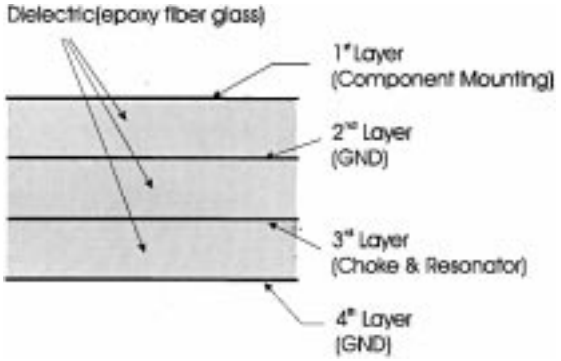

Fig. 2. Sectional view of the multilayer PCB.

One of the key features of the circuit in Fig. 3 is in reduction of the dc current by having two transistors share the same emitter current. In this configuration, the output power may be reduced because it limits the output voltage swing. However, the required power is usually small, typically about 0 dBm. Thus, reduction in the dc current may become a key requirement of the VCO's for mobile-communication handsets. The circuit in Fig. 3 achieves low dc-current consumption and meets all the other VCO requirements. Thus, it is highly probable that the VCO circuit in Fig. 3 will be used in next-generation high-frequency mobile-communication systems.

This paper deals with transistor selection for the VCO circuit of Fig. 3 used in next-generation high-frequency mobile communication. One of the conventional approaches is to choose a silicon bipolar junction transistor (BJT) having the maximum frequency of oscillation $f_{\max} = \sqrt{f_T/(8\pi r_{bb'} C_{ob})}$ even if it is higher than required. It was found, however, that it is necessary to choose the BJT's much

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The author is with the Department of Radio Sciences and Engineering, College of Engineering, Chungnam National University, Taejeon, Korea.

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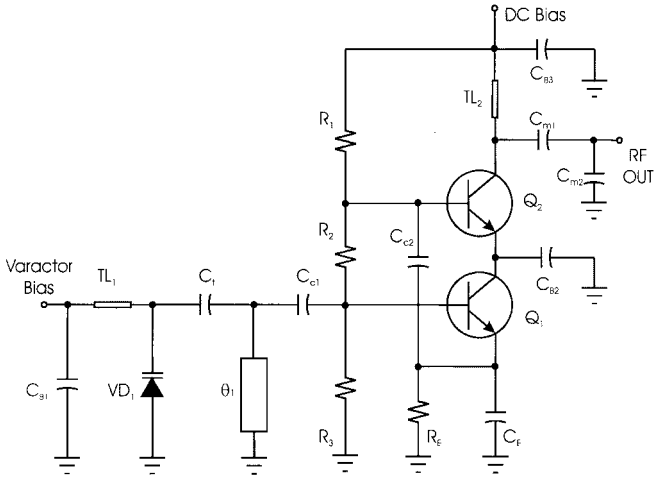

Fig. 3. Typical commercial VCO circuit used in the 900-MHz mobile-communication handset.

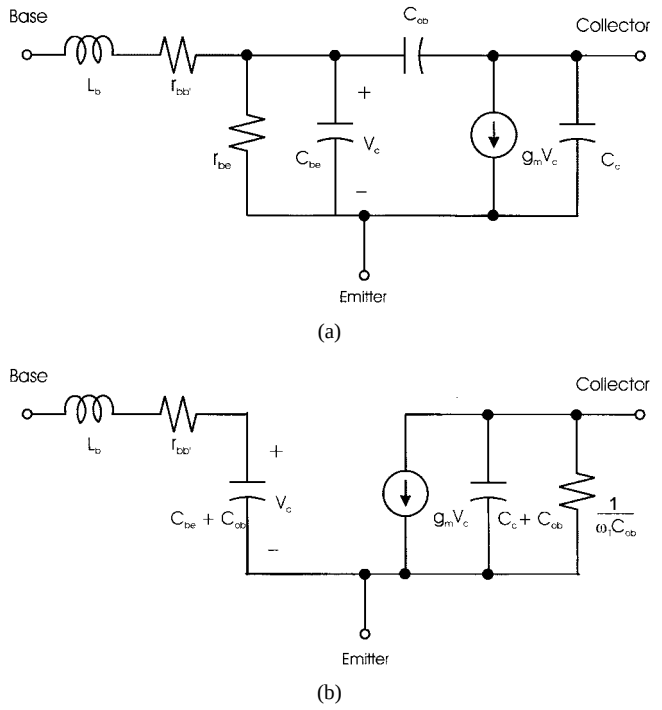

Fig. 4. (a) Small-signal equivalent circuit of BJT. (b) Approximate unilateral small-signal equivalent circuit.

higher than the expected $f_{\max}$ because of the effects of other circuit elements.

II. Analysis of the VCO Circuit

In Fig. 3, the capacitors C_{B1}, C_{B2}, and C_{B3} are bypass capacitors. The voltage across capacitor C_{B1} is used for tuning the varactor VD_1. The dc voltage across the capacitor C_{B3} is for dc-biasing transistors Q_1 and Q_2. The capacitor C_{B2} provides the ac ground for both the transistors Q_1 and Q_2. Thus, the transistors Q_1 and Q_2 are in the common collector and emitter configuration, respectively. The feedback capacitor C_E makes the transistor Q_1 unstable. Thus, the real part of the impedance seen from the resonator θ_1 becomes negative.

To obtain the negative resistance seen from the resonator, the small-signal equivalent circuit of the silicon BJT, as shown in Fig. 4(a), is required. The equivalent circuit can be replaced by the approximate unilateral equivalent circuit in Fig. 4(b) because C_{ob} is small. In Fig. 4(b), ω_T is the angular cutoff frequency defined by $\omega_T = 2\pi f_T = g_m/C_{be}$. The resistor $1/\omega_T C_{ob}$ is inserted to represent the real part of the y_{22} of the equivalent circuit at the high-frequency limit. To put the unilateral equivalent circuit into the circuit of Fig. 3, one can redraw the circuit, as shown in Fig. 5. Subscript 2 is added to the equivalent-circuit elements in order to distinguish them from those of Q_1. Both R_{eq} and C_{eq} in Fig. 5 are given by

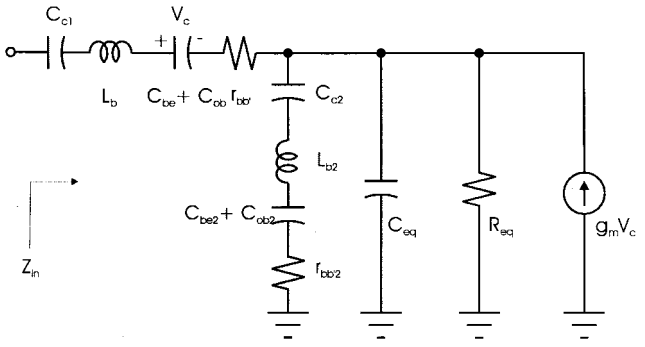

Fig. 5. RF small-signal equivalent circuit seen from the resonator for the calculation of the negative resistance.

$$R_{eq} = R_E \left\| \frac{1}{\omega_T C_{ob}} \right. \tag{1}$$

$$C_{eq} = C_c + C_{ob} + C_E. \tag{2}$$

In this circuit, the $r_{bb'2} - L_{b2} - C_{c2}$ branch represents the loading of Q_2. This branch can be absorbed into (1) and (2) through the series parallel conversion. The real part due to $r_{bb'2}$ will be added in parallel to the resistance R_{eq} in (1), and will lead to the decreased R_{eq}. The imaginary part will be added in parallel to the capacitance C_{eq} in (2). Thus, without the loss of generality, this circuit can be analyzed without this branch.

With C_{c2} set to zero, Z_{in} can be written as

$$Z_{\text{in}} \approx r_{bb'} + j\omega L_b + \frac{1}{j\omega(C_{ob} \| C_{c1})} + \left(1 + \frac{g_m}{j\omega C_{be}}\right) \frac{R_{eq}}{1 + j\omega C_{eq} R_{eq}}. \tag{3}$$

Taking the real part of Z_{in} and computing the angular frequency ω_c, which makes the real part zero, will be given by

$$\omega_c^2 = \frac{2\pi f_T k x - k\left(1 + \frac{1}{k}\right)}{x^2} \tag{4}$$

where $x = C_{eq} R_{eq}$ and $k = R_{eq}/r_{bb'}$. From (4), ω_c^2 can be maximized by adjusting the external circuit element C_E and R_E. For a given R_E, if C_E is adjusted for the maximum of ω_c^2, the maximum oscillation frequency $\omega_{c,\max} = 2\pi f_{c,\max}$ can be obtained as

$$f_{c,\max} = \frac{f_T}{2} \sqrt{\frac{k}{1 + \frac{1}{k}}} \approx \frac{f_T}{2} \sqrt{\frac{R_{eq}}{r_{bb'}}}. \tag{5}$$

The $f_{c,\max}$ in (5) can be considered as the maximum frequency of oscillation of the presented VCO circuit. As R_E approaches infinity, it can be found that $f_{c,\max}$ will approach the well-known $f_{\max}$, the maximum frequency of oscillation of the transistor itself [4] given by

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r_{bb'} C_{ob}}}. \tag{6}$$

It may also be necessary to consider the negative-resistance margin to cancel out the resistance resulting from the resonator and the

TABLE I
$f_{p,\max}$, $f_{c,\max}$, AND THE RESULTS OBTAINED DIRECTLY FROM THE MEASURED TWO-PORT S-PARAMETERS

Device Part No.	$f_{p,max}$[GHz] R_E=100	$f_{c,max}$[GHz] R_E=100	f_{max}[GHz]	f_{osc_S}[GHz]	f_{max_S}[GHz]
NE68019	**2.6**	**3.7**	**4.9**	**2.9**	**4.2**
NE68119	**2.1**	**3.0**	**4.2**	**2.3**	**3.9**
NE85619	**1.5**	**2.1**	**2.9**	**1.5**	**4.4**
NE85630	**1.2**	**1.7**	**2.2**	**1.1**	**2.4**
NE94433	**0.7**	**1.1**	**1.6**	**0.6**	**1.2**

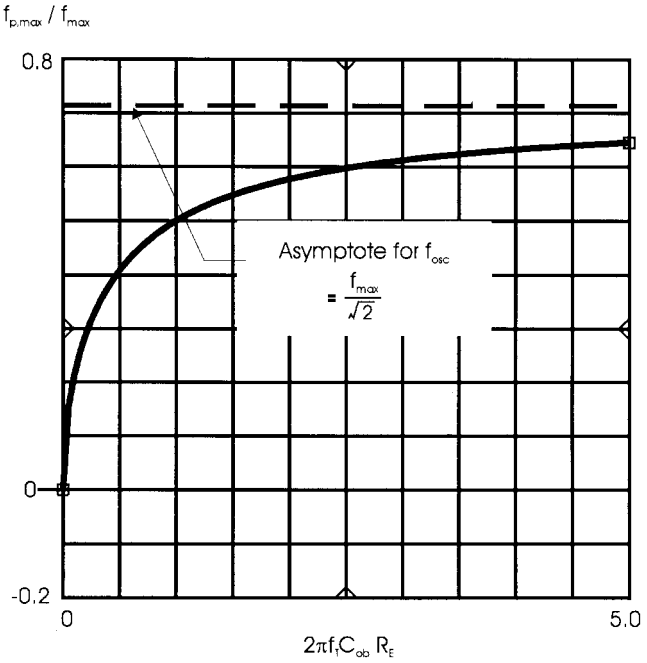

Fig. 6. $f_{p,\max}$ versus R_E ($f_{p,\max}$ is normalized by $f_{\max}$ and R_E is normalized by $1/2\pi f_T C_{ob}$).

varactor. This margin may be obtained if the proper backoff constant is determined from $f_{c,\max}$. Here, the backoff constant is set as $1/\sqrt{2}$. With this backoff constant, the practical maximum frequency of oscillation is given by

$$f_{p,\max} = \frac{f_T}{2}\sqrt{\frac{R_{eq}}{2r_{bb'}}}. \tag{7}$$

If we replace $r_{bb'}$ in (3) by $2r_{bb'}$, $f_{c,\max}$ will become $f_{p,\max}$, considering the change of k in (5). Thus, $f_{p,\max}$ is, in another sense, the frequency maximum where the real part of Z_{in} becomes equal to $-r_{bb'}$. The proposed backoff $1/\sqrt{2}$ from the $f_{c,\max}$ will give the negative resistance margin of $r_{bb'}$, which is required to build up the oscillation.

By neglecting the loading of transistor Q_2, (7) can be written as

$$f_{p,\max} = \frac{f_{\max}}{\sqrt{2}}\sqrt{\frac{R_E}{R_E + \dfrac{1}{2\pi f_T C_{ob}}}}. \tag{8}$$

Four parameters (f_T, $f_{\max}$, C_{ob}, and R_E) are required in computing $f_{p,\max}$. Among these four parameters, the three parameters f_T, $f_{\max}$, and C_{ob} are basically determined by the device itself. Thus, the emitter resistor R_E can be thought of as the true design parameter available. R_E dependence of the normalized oscillation frequency $f_{p,\max}/f_{\max}$ is plotted in Fig. 6. The plot shows that as the R_E becomes larger, $f_{p,\max}$ approaches $f_{\max}/\sqrt{2}$, the maximum frequency of oscillation of the device itself with backoff. It is pointed out that in the region of small R_E, the normalized $f_{p,\max}$ decreases very rapidly as R_E decreases.

The significantly decreased $f_{p,\max}$ with a small R_E will lead to a serious problem in designing the presented VCO circuit, especially for a low-voltage operation. For example, when the supply voltage is 3–5 V, the maximum voltage drop across R_E may be only 0.5–1.0 V. The small allowable voltage drop can be achieved only by choosing a small R_E and, in turn, will inevitably lead to a seriously decreased $f_{p,\max}$. Thus, for the presented VCO circuit, a transistor with much higher (than usually estimated) $f_{\max}$ should be chosen.

III. THE VERIFICATION OF THE FORMULA

$f_{p,\max}$ may be computed in two ways using measured S-parameters for the selected device. One is replacing the transistors by the given small-signal S-parameters. For a given C_E, the frequency can be found where the negative resistance seen from the resonator is equal to $-r_{bb'}$. The frequency will change with respect to the change of C_E. $f_{p,\max}$ will then be the maximum of the frequencies with respect to C_E. The resulting $f_{p,\max}$ is exact, supported by the measurements alone, and may be used as the criterion to determine the accuracy of (7). The other approach is to obtain the unilateral equivalent circuit from the measured two-port S-parameters and to compute $f_{p,\max}$ by inserting the element values into (8).

From the unilateral equivalent circuit, $r_{bb'}$ can be found as

$$r_{bb'} = \text{Re}\left(\frac{1}{y_{11}}\right). \tag{9}$$

On the other hand, by plotting the imaginary part of $1/y_{11}$ as a function of frequency, the series resonance may be easily found. Near the resonance, the slope will be estimated and equated to $2L_b$. The L_b is then obtained by calculating the slope using the relation as

$$X \approx 2L_b(\omega - \omega_o) \approx \text{Im}\left(\frac{1}{y_{11}}\right). \tag{10}$$

A new two-port can be obtained by connecting the negative-valued $r_{bb'}$ and L_b in series to the input of the transistor. The negative $r_{bb'}$ and L_b cancel out the positive $r_{bb'}$ and L_b in Fig. 4(a), and the resulting equivalent circuit will have a π-structure. If we denote Y-parameters for the new two-port as Y', the other element values can be obtained by matching the resulting π-circuit to the

π-equivalent representation [5] of the new Y'-parameters as [6]

$$C_{ob} = \frac{\mathrm{Im}(-y'_{12})}{\omega} \tag{11}$$

$$C_{be} = \frac{1}{\omega}\mathrm{Im}(y'_{11} + y'_{12}) \tag{12}$$

$$g_m = |y'_{21} - y'_{12}|. \tag{13}$$

Finally, both $f_{c,\max}$ and $f_{p,\max}$ are calculated by inserting the elements values obtained from (9) to (13) into (5) and (8).

In Table I, both $f_{c,\max}$ and $f_{p,\max}$ are computed with $R_E = 100\ \Omega$ in the first two columns. The transistors are biased to $V_{CE} = 2.5$ V and $I_E = 3$ mA and packaged with low-cost plastic-mold types.[1] For comparison, the results obtained from S-parameters are also summarized in the last two columns $f_{\max\_S}$ and f_{osc_S}, respectively. As compared in Table I, $f_{p,\max}$ is in relatively good agreement with f_{osc_S}, but the estimated $f_{c,\max}$ needs some further improvements. The discrepancy between $f_{c,\max}$ and $f_{\max\_S}$ may be from the fact that the small-signal equivalent circuit [as in Fig. 4(a)] does not represent the measured S-parameters very well near the frequency $f_{\max}$. It is also shown in Table I that to apply this VCO circuit at 2 GHz, transistors with $f_{\max}$ higher than 4 GHz are required.

IV. Conclusion

For the presented VCO circuit, new formulas for estimating the maximum frequency of oscillation were developed. $f_{p,\max}$ shows the strong dependence on the emitter bias resistor in the region of small R_E, which greatly reduces the oscillation capability of the transistor itself. To prevent the degradation, the voltage drop across the emitter resistor should not be set so small. The formulas can be used as a practical guide in choosing the active devices for the presented VCO circuit.

The validity of the formula is verified by comparing the results with those obtained from replacing the transistors by the measured two-port S-parameters. The comparison shows that $f_{p,\max}$ computed from the unilateral equivalent circuit is in good agreement with that obtained from the S-parameters. For the given R_E, the $f_{p,\max}$ computation with an equivalent circuit is somewhat tedious compared with the direct S-parameter replacement. However, if done, one may find that the proper R_E does not significantly degrade the oscillation capability for the chosen device. In addition, it can be determined whether or not the chosen device is adequate for the presented structure at a given supply voltage.

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A New Approach to Nonlinear Analysis of Noise Behavior of Synchronized Oscillators and Analog-Frequency Dividers

J. C. Nallatamby, M. Prigent, J. C. Sarkissian, R. Quere, and J. Obregon

***Abstract*—An original theory of phase noise in synchronized oscillators is outlined through the phase-locked loop (PLL) approach. The phase-noise spectrum obtained first by the analytical PLL theory and then by the simulator developed in [1] have been compared with very good accuracy. This new approach permits the best understanding of noise conversion in synchronized devices.**

I. Introduction

The purpose of this paper is to outline a new approach to nonlinear analysis of noise behavior in potentially unstable circuits such as synchronized oscillators. The nonlinear noise theory for synchronized oscillators has been given by Schunemann [1]. Goedbloed and Vlaardingerbroek [2] calculated the transfer properties of the injection-locked oscillator. However, [1] and [2] give a good qualitative understanding of the noise behavior for the fundamentally synchronized oscillator only. A general expression for output FM noise calculation for subharmonic injection-locked oscillators was formulated in terms of injected phase noise, intrinsic noise of the free-running oscillator, and the injection locking range [3]. A complementary study with previous works and an original approach to evaluate noise in the injection-locking mechanism of an oscillator by the help of the analog phase-locked loop (PLL) theory will be discussed in detail. The phase-noise spectrum analytically obtained by the PLL approach is compared with the results of the nonlinear noise simulator developed in [4].

II. Noise in Synchronized Oscillator

Let us consider a Van Der Pol oscillator, shown in Fig. 1. A parallel resonant circuit (RLC) approximates the resonance structure. The voltage source $e(t)$ represents an intrinsic noise generator where the spectral density which varies with the law $\langle E(f)^2\rangle = (1e-9)/f$. $i_s(t)$ is the synchronizing current source. The active device is modeled by two elements with the Van Der Pol third-order polynomial characteristic

$$i(v) = b \cdot v + d \cdot v^3, \qquad \text{with } b = -0.02 \text{ and } d = 0.7\ q(v) = q_0 v. \tag{1}$$

This gives us a good understanding of the oscillator noise behavior because it contains the main nonlinearities of all transistor nonlinear models (MESFET, bipolar, heterojuction bipolar transistor (HBT), ...). We are now in a position to analytically calculate the contributions to the output noise spectrum due to both the intrinsic noise source $e(t)$ and to the injected current source $i_s(t)$.

A. Effects of Injected Noise

The noise sources considered here concern only the phase noise of the injection signal. It is possible to describe the noise of a synchronized oscillator via the analogy of phase-locking mechanism.

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The authors are with IRCOM-UMR CNRS 6615, 19100 Brive, France.
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